Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-14. (Previously Cancelled)

15. (Currently Amended) A method of manufacturing a semiconductor device comprising ~~the steps of~~:

forming an etching mask constituted by a first insulating film having an opening portion including a gate forming portion and source/drain extension regions forming portion on a surface of a semiconductor substrate;

forming a trench in the semiconductor substrate in correspondence with the opening portion of the etching mask;

forming a gate insulating film constituted by a second insulating film on an inner surface of the trench;

forming a gate material film on the second insulating film;

patterning the gate material film to form a gate on a central portion between both sides of the trench on a source/drain side through the second insulating film, while providing an exposed bottom surface of the trench between the central portion and both sides of the trench, on which the gate material film does not exist;

implanting impurity ions into at least ~~a~~ the exposed bottom surface of the trench by using the entire gate as a mask to form source/drain extension regions;

forming a third insulating film to cover the surface of the semiconductor substrate;

forming gate sidewall spacers constituted by the third insulating film by using anisotropic etching to cover the inner surface of the trench extending on the source/drain side of the gate; and

implanting impurity ions into the source/drain regions by using the gate having the gate sidewall spacers as a mask to form a MIS-type field effect transistor having source/drain regions being close to or adjacent to side surfaces of the trench of the semiconductor substrate and connected to the source/ drain extension regions on the bottom surface of the trench in which a position where an impurity concentration of the source/drain regions in the direction of depth is maximum ~~almost~~ substantially coincides with a position where an impurity concentration of the source/drain extension regions in the direction of depth is maximum.

16. (Previously Amended) A method of manufacturing a semiconductor device according to claim 15, wherein the trench is formed by isotropic etching such that the side surfaces of the trench on the source/drain side constitute a rounded surface.

17. (Previously Amended) A method of manufacturing a semiconductor device according to claim 15, wherein ion implantation for threshold voltage control of the MIS-type field effect transistor is performed to only the bottom surface of the trench.

18. (Previously Amended) A method of manufacturing a semiconductor device according to claim 15, wherein the first, second, and third insulating films are an SiO_2 film formed by an LPCVD method using TEAS, an SiO_2 film formed by thermal oxidation of silicon, and an SiN film formed by a CVD method, respectively.

19. (Previously Amended) A method of manufacturing a semiconductor device according to claim 15, wherein the first insulating film is formed to be stacked on a thermal oxidation film formed as a buffer layer on the semiconductor substrate.

20. (Previously Amended) A method of manufacturing a semiconductor device according to claim 15, further comprising after a silicide film of high melting point metal is formed on a silicon surface exposed to the source/drain regions and upper surfaces of the gate consisting of polysilicon by forming a high melting point metal film to cover the surface of the semiconductor substrate and performing heat treatment, removing the high melting point metal film remaining on the gate sidewall spacers.

21-34 (Previously Cancelled)

35. (Currently Amended) A method of manufacturing a semiconductor device ~~according to claim 15~~ comprising:

forming an etching mask constituted by a first insulating film having an opening portion including a gate forming portion and source/drain extension regions forming portion on a surface of a semiconductor substrate;

forming a trench in the semiconductor substrate in correspondence with the opening portion of the etching mask;

forming a gate insulating film constituted by a second insulating film on an inner surface of the trench;

forming a gate material film on the second insulating film;

patterning the gate material film to form a gate on a central portion between both sides of the trench on a source/drain side through the second insulating film;

implanting impurity ions into at least a bottom surface of the trench by using the gate as a mask to form source/drain extension regions;

forming a third insulating film to cover the surface of the semiconductor substrate;

forming gate sidewall spacers constituted by *the* third insulating film by using anisotropic etching to cover the inner surface of the trench extending on the source/drain side of the gate; and

implanting impurity ions into the source/drain regions by using the gate having the gate sidewall spacers as a mask to form a MIS-type field effect transistor having source/drain regions being close to or adjacent to side surfaces of the trench of the semiconductor substrate and connected to the source/ drain extension regions on the bottom surface of the trench, in which a position where an impurity concentration of the source/drain regions in the direction of depth is maximum substantially coincides with a position where an impurity concentration of the source/drain extension regions in the direction of depth is maximum,

wherein an allowable misfit range required to make the maximum positions coincide with each other is about $\pm$ 0.01 μm with respect to the conditions for perfect coincidence.